Susceptibility of ICs to Conducted Electromagnetic Interference

Ognjen Jović

Department of Engineering Integrated Circuits Methods, Tools and Technologies
Robert Bosch GmbH (AE/EIM), Germany
Ognjen.Jovic@de.bosch.com

Abstract—This work is focused on the susceptibility of integrated circuits (ICs) to electromagnetic interference (EMI). The main issue is simulation and measurement on device level and circuit level. The work gives an overview of the overall electromagnetic compatibility (EMC) issues, and shows Direct Power Injection (DPI) measurement technique for conducted electromagnetic interference. Related research that is concerned with simulations, measurements and improvement of ICs against EMI is presented. Finally future work and concepts are discussed.

I. INTRODUCTION

One of the most difficult challenges today, especially for the very demanding automotive market, is to improve design methodology and develop modelling techniques that can provide realistic simulations of circuit performance. It is imperative to assess electromagnetic incompatibilities at an early stage in order to reduce overall design cost and time-to-market, as well as to improve reliability and performance.

The performance of ICs is consistently rising since the invention of the first IC. The progress in semiconductor technologies allows higher integration of interfaces, boosted switching speeds, and lower power supplies as shown in Fig. 1 and Fig. 2. Three voltage trends can be seen (see Fig. 2): the input-output (IO) voltage tends to be reduced step-by-step (5 V – 1.8 V), the core supply which has decreased from 5 V to 1 V in 90 nm, and the associated noise margin has been cut by a factor of 10 [1].

The consequence of growing electronic appliances due to semiconductor technologies is increased radio frequency (RF) emission and susceptibility of the ICs to radiated and conducted perturbation.

Fig. 1. Microprocessor and microcontroller frequency increase [1]

Fig. 2. Continuous decrease in supply voltage [1]

Electromagnetic environment in motor vehicles generated by devices like ABS braking systems, alternator, ignition system, switching solenoids, electric starter, or lamps is extremely complex. Without a proper design which is EMC aware, performance of integrated circuits will become a limiting factor in the performance of every advanced electronic system.
The continuous and constant increase of the number of electronic devices on vehicles has brought automotive products to fulfil very harsh EMC requirements, both for electromagnetic immunity and electromagnetic emission. This is even more severe on power train and safety products [2].

To cope with EMC threats and avoid cost consuming redesigns of ICs, the EMC design should be incorporated in the overall IC design flow [3]. Therefore, both IC vendors and customers need proper models to forecast the susceptibility of their products.

The main focus of this work is the susceptibility of ICs to electromagnetic interference. From the EMC point of view it is clear that an IC alone cannot give reliable results for the whole system. However, the robustness and reliability of ICs is the first and mandatory step to reach reliable system performance.

In section II the EMC overview is presented. A non exhaustive illustration of present research of integrated circuits susceptibility to EMI is provided in section III. Direct power injection measurement technique to perform EMI tests of ICs is shown in section IV. Section V outlines further work and discusses possible improvements. Finally, the conclusions are presented.

II. EMC OVERVIEW

A. Aspects of EMC

Electromagnetic compatibility is concerned with the generation, transmission, and reception of electromagnetic energy as illustrated in Fig. 3. These three aspects of EMC problem form the basic framework of any EMC design. The source (emitter) produces the emission, and a transfer or coupling path transfers the emission energy to a receptor, where it is processed, resulting in either desired or undesired behaviour [4].

Interference occurs if the received energy causes the receptor to behave in an undesired manner. Transfer of electromagnetic energy occurs frequently via unintended coupling paths. However, this unintended transfer of energy causes interference only if the received energy is of sufficient magnitude (energy) and/or spectral content at the receptor input to cause the receptor to behave in undesired fashion [4].

There are three ways to prevent interference:

1. Suppress the emission at its source.
2. Make the coupling path as inefficient as possible.
3. Make the receptor less susceptible to the emission.

The transfer of electromagnetic energy can be divided into four subgroups: radiated emission, radiated susceptibility, conducted emission, and conducted susceptibility as depicted in Fig. 4.

Electromagnetic emissions can occur from the ac power cord, a metallic enclosure containing a subsystem, or from an electronic component within a non-metallic enclosure. It is important to keep in mind that currents radiate. A time varying current is the essential way of producing radiated emission. The longer the cable the more efficient will be the emitting and/or picking up of the electromagnetic energy.

Emissions of and susceptibility to electromagnetic energy occur not only by electromagnetic waves propagating through air but also by direct conduction on metallic conductors, or power supply lines. Usually this coupling path is more efficient than the air coupling path.

![Figure 4. Four basic EMC situations](image)

The interfering signal propagates mainly in two different ways: radiation and conduction (Fig. 4). Due to small chip dimensions and relatively low frequencies at which most circuits are operating, the conduction presently seems to be the most relevant way of propagation.

The chip dimensions are measured in wavelengths. Typically used criterion is that a circuit is electrically small when the largest dimension is smaller then one-tenth of electromagnetic wavelength at the largest frequency components.

B. History of EMC

Radio interference from an electrical apparatus, such as electric motors, electric railroads, and electric signs began to appear as a major problem around 1930. However, the most significant increase of the interference problem occurred with the inventions of high-density electronic components such as the bipolar transistor in the 1950s, the integrated circuit in the 1960s, and the microprocessor chip in the 1970s [4]. The density of noise sources rich in spectra content (switching waveforms) has become quite large. Consequently, the
occurrence of electromagnetic immunity problems began to rise.

Most of the EMC activity during the 1960 to 1980 period was spent on cable coupling, grounding-shielding and power line transients. Around 1975 an increased share of EMC has been devoted to PCB level issues. Finally, beginning at 1990, EMC analysis and solutions at the IC level did their progressive entry in the regular electronic design circles [5].

With smart power technology, that has started with junction isolated techniques, the implementation of power devices and control units on the same chip becomes possible. This technology is suited for many applications including household appliances and automotive domain. The main concern of such compact circuits, especially in automotive industry due to cost effective solutions and high reliability requirements, is the strong electrical interaction between the power device and sensitive analogue circuitry on the same chip.

III. INVESTIGATION OF EMI AT IC LEVEL

The effects of an electromagnetic wave coupling to PCB traces and the consequences of this coupling on simple circuits is analysed in 1995 by Laurin [6], [7]. In 1997, Chappel has discussed the possibility of hardening integrated circuits to electromagnetic interference by specific design techniques that raised the immunity level of ICs. Several other circuits have also been proposed that exhibit a high immunity to RFI, including Schmidt triggers, low-voltage differential swing circuits and delay-insensitive circuits. In 2000, an updated version of the Integrated Circuit Electromagnetic Immunity Handbook published by NASA gave valuable information on the immunity levels of simple integrated circuits up to 10 GHz [8], [7].

Further investigations have also been concerned with operation point shift of a single transistor like nMOSFET, when a large RF signal is injected into gate and drain [9]. Hattori has shown that, when an RF signal is injected at the gate, the drain current increases in the saturation region, changes in the linear region, and a negative drain current flows near $V_D = 0$ V. If an RF signal is injected into the drain, a large negative drain current flows near $V_D = 0$ V. Using SPICE LEVEL 3 as the MOSFET model and adding an additional parasitic resistance of the bulk, the effect of large negative current flow at $V_D = 0$, when a large RF signal is injected into the drain, can be simulated.

Another investigation of transistor model has been published by Fiori in [10]. The Gummel-Poon (GP) model of a bipolar transistor has been improved in the sense that it takes into account distributed phenomena excited by RF interference like the dc and ac crowding of the emitter current in the base region. The predictions of a new model have shown a good agreement with experimental results.

Besides a single transistor case, investigations have also been focused on more complex circuits: bandgap, operational amplifier, and regulators [11] – [20].

It is well known that one of the most susceptible circuits to RF noise is the operational amplifier. One of the undesirable effects of interference is a shift of the output DC mean value (DC offset) that might force the amplifier, or subsequent stage, into saturation. The susceptibility of this circuit is highlighted in several studies [11] – [13], where some possible explanations, e.g. slew-rate asymmetry, distortion phenomena related to the differential pair are pointed out. In the same way strongly symmetric topologies with cross-coupled amplifiers with active loads, as well as frequency selective input differential stages have shown a higher immunity to RF disturbance [14], [15].

Similar analysis is also done on another fundamental analogue block of an IC, the bandgap voltage reference whose precision can influence for example the proper functionality of the regulator, or AD (DA) converters integrated on the same chip. Most studies are concerned on the operational amplifier which is inherently embedded in the most common bandgap topologies [16], [17]. But, even with highly immune operational amplifiers the overall bandgap circuit could be made useless if the specific bandgap cell is not considered and optimised as well [18], [19]. Investigations have also been focused on design rules for bandgap circuits, operational amplifier [20], and CAN receiver [21]. The proposed techniques are to limit incoming EMI signal by using low pass filters or capacitive loads.

More recently, investigations have been focused on local interconnect network (LIN) output driver that is low speed (max. transmission speed is 20 kb/s) serial communication protocol primarily used in cars, and a dc current regulator with solutions to improve the immunity to EMI [22], [23].

Another important issue in EMC is surely simulation time of the IC performance. The simulation time is rising rapidly with the complexity of the circuits especially if performing time domain simulations. To reduce simulation time frequency domain analysis can be used [24], [25]. Admittedly, up to some complexity level convergence problems will occur and some additional solutions have to be found. One of those solutions is to use a macro model of the circuit [26] – [28], or a model that embeds a whole system like measurement setup with integrated circuit and its environment [29].

IV. DPI MEASUREMENT

A. DPI measurement of ICs

Up to now, the most appropriate method for conducted susceptibility measurements of an IC is the Direct Power Injection (DPI). This method is well described in standard IEC 62132-4 [30]. It is pin selective and interfering signals can be easily reproduced by a signal generator. Fig. 5 depicts typical measurement setup for a DPI test.

The RF disturbance is a continuous sinusoidal waveform with frequency of 150 kHz up to 1 GHz, or amplitude modulated signal (1 kHz with 80% for the modulation factor). The usual power limit is 1 W or 30 dBm. The level could reach 5 W (37 dBm) for specific applications. The signal generated by RF generator is injected on the pin of an IC through a decoupling block (BiasTee). Usually the DC block is realized by a capacitor and inductor to decouple the AC
signal from the DC. The signal is forwarded through the amplifier to the directional coupler were forward and reflected power are measured. The directional coupler builds together with signal generator and amplifier a closed loop that adjusts correct forward power at every frequency point. For the adjustment only the forward power is important. The correction is necessary to compensate possible losses and reflections on the line that could alternate the amplitude of the forwarded signal.

To reduce reflections, it is strongly recommended to adapt the setup in the way to have a 50 Ω characteristic wave impedance from the RF generator to the DUT. Also to avoid taking into account the cable effects, an optional attenuator (commonly 3 dB or 6 dB) may be inserted just before the decoupling block, which features a 50 Ω–input impedance.

The measurement algorithm for standard DPI is depicted in Fig. 6.

**B. DPI Measurement on wafer**

DPI measurement on wafer level differs from the typical DPI approach in the way that uses specially designed high frequency (HF) probes to assure contact on wafer as depicted in Fig. 7. In this way the spurious effects from package of IC like bond wires, lead frames and traces of test board are avoided.

This type of measurement enables direct validation of an IC, granted that the measurement set-up is calibrated in advance.

The test structures have to be adopted in the way to allow such type of measurement, and the contact pads should be designed for ground-signal-ground HF probes. To avoid reflections on cables, it is recommended to terminate all signal paths with 50 Ω loads.

![Figure 7. HF probes connected on specially designed HF pads](image.png)

**V. FURTHER WORK**

Despite the work reported in previous section, a lot of space is still left for research and improvement in analogue circuit design.

Due to rising EMC requirements, one of the uncertainties in automotive industry is the validity of simulation models. Commonly the most used transistor models in automotive industry are sub-circuit based Gummel-Poon for bipolar and BSIM3 for MOSFET transistors. Till now all high voltage transistors are modelled as sub-circuits, which, depending on different supplier and requirements of customer, differ from each other. Therefore it is hard to say how good these models are. In a view of EMI there is a still lack of validated simulations for smart power technologies.

In almost the same manner, the precautions used by an IC designer to improve the electromagnetic immunity of the circuit should be better defined.

Subtopics for further investigations in order to improve the susceptibility predictions as well as to give valuable hints to IC designers are:
1. Physical understanding of the effects that are occurring in a single transistors and higher complexity circuits when exposed to large RFI by wide band excitation.

2. Optimisation techniques that can be widely used, e.g. of transistor models (parameters) or circuits to improve their immunity to EMI.

3. Validation of more complex circuits (current mirror, bandgap, regulator) in smart power technology in a view of susceptibility predictions to EMI.

4. Extension of EMI simulation to detect sensitive elements in early stage.

A. Concept to investigate effects of EMI and validate simulation models of single transistors and higher complexity circuits in smart power technology

Investigations of EMI at transistor level (mostly high voltage transistors) and circuits like high-voltage current mirror, bandgap or regulator, are possible with special test structures that have been designed in smart power BCD technology. The test structures are available on wafer, and due to carefully designed pads it is possible to conduct DPI measurements at IC level.

Simulations are preformed in Cadence Design Environment with Spectre simulator [31]. Used models are BSIM3v3 for MOSFET and Gummel-Poon for bipolar transistors. The control of simulation and validation of results is done by Matlab [32].

Measured results are used as reference to which the simulations are compared. If the accuracy of simulation models is not sufficient, further optimisations, as shown in Fig. 8, can be derived.

![Figure 8: Example of time domain measurement and simulation of the output signal V_{OUT2} of PMOS transistor with original and improved sub-circuit model](image)

B. Concept of optimisation technique to optimise transistor parameters

Optimisation of transistor parameters is performed with Matlab by using evolutionary strategy [33]. It enables DC and time domain optimisations, where simulation results are compared with measurements. This method should not replace commercial available tools like integrated circuit characterisation and analysis program IC-CAP that provides among other things optimisation of transistor models. The Matlab methodology is more proper for enhancement in the sense to use optimisation techniques necessary for larger circuits. The program flow is depicted in Fig. 9.

![Figure 9: Program flow for parameter optimisation](image)

C. Extension of EMI simulation to detect sensitive elements in early stage

An IC designer has to face EMC requirement in an early stage of design. Mostly, the experience of the IC designer is a crucial factor for a correct circuit design in view of EMI. However, sometimes due to complexity of the circuit and shortage of time, it is not always possible to localize sensitive elements of the design and that can impair the immunity of the whole circuit. Therefore it would be a great benefit to add in the standard simulation environment a tool for automatic detection, or at least automatic localisation of the circuit parts that show higher sensitivity to EMI.

Such a feature could be implemented through Matlab. The IC designer would use a script that is written in Matlab. All settings important for simulation, e.g. stabilisation time, number of periods, simulation method and so on, could be adjusted by the designer. The Matlab would start the simulation and according to data evaluation method the sensitive nodes would be written in a standard file with corresponding voltages and currents that showed the highest offset comparing to DC values.
VI. CONCLUSION

This work gives a short introduction to EMC at chip level and shows an overview of the research during the past years that is concerned with susceptibility of the ICs to EMI. The direct power injection method is explained and on wafer measurements are illustrated.

Nowadays the robust IC design is a mandatory factor to fulfill high EMC requirements, especially in automotive domain, due to harsh operating environment and cost effective solutions.

One of the uncertainties in automotive industry is the validity of simulation models in smart power technology. Most simulation models (especially high voltage transistors) are sub-circuit based.

Depending on different supplier and requirements of customer, these models can differ from each other. In a view of EMI there is still a lack of validated simulations for smart power technologies.

The concept to validate and improve simulation models/circuits in smart power technology is presented, and suggested extension of EMI simulation to detect sensitive models/circuits in smart power technology is proposed.

REFERENCES


