FPGA based hardware acceleration of dynamic phasor estimation algorithm

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1. Introduction

Modern electrical grid is changing.
- Renewables,
- Distributed generation
- E-charging
- Battery storage
- Power electronics

Monitoring the grid is more challenging than before
Traditional concepts:
- One-directional energy flow
- SCADA, Phasor measurement units (PMU)

We are witnessing many power outages all over the world which sometimes kick whole countries off the grid.

2. Problem Description

Common phasor estimation techniques usually deal with stationary states. Their inherent reliance on Discrete Fourier Transformation (DFT) leads to poor performance in dynamic conditions. Measurement standards leave much larger error tolerances for transient conditions, even though they are crucial for understanding modern grid state. Many calculations must be made in short time, with reporting rate up to 50 times per second.
Parametric estimation techniques such have recently gained popularity [1]. Electric signal can be modeled as a sum of complex signals, and if model order is known, good results can be achieved. Parameters of a phasor can be dynamic, and contain harmonics and interharmonics.

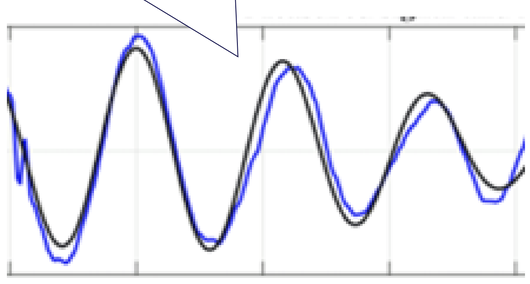
3. Methodology

After signal acquisition, complex number matrix is prepared for ESPRIT parameter estimation.
Autocorrelation matrix is formed and model order is evaluated.

Dynamic phasor model performance is tested in MATLAB, by reconstructing some common transient grid conditions.
- Measured signal (blue) vs.
- Reconstructed signal (black)

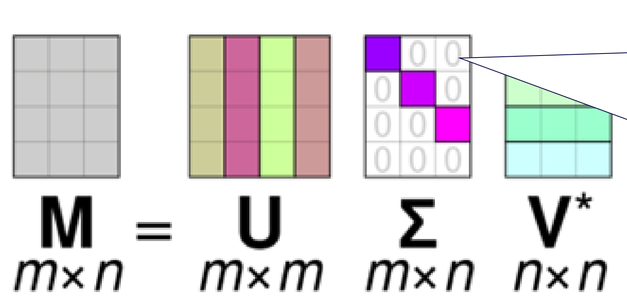
Electric signal is modelled as a sum of:
- Main signal
- Harmonics and interharmonics
- Exponentially damped components,

rendering complex number signal representation



Recostruction of measured signal

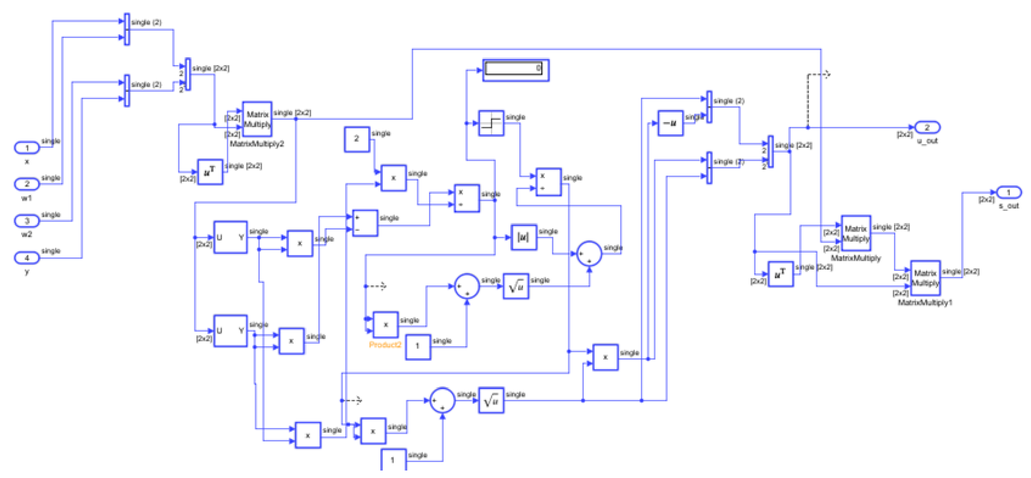
Crucial and computationally most intensive part of the ESPRIT diagram is the signular value decomposition (SVD). After signal acquisition, matrix is formed and decomposed.



There are several matrix decomposition algorithms. Commonly used one-sided Jacobi Hestenes algorithm allows parallelization, which is suitable for FPGA implementation. [2]
Matrix decomposition can be performed by splitting the problem in 2x2 matrices. As the next step, both algorithm and model are implemented using High Level Synthesis (HLS) in MATLAB. Matrix decomposition problem is improved using neural networks rather than classical CORDIC based iterative approach.

4. Results

Proposed dynamic phasor model accurately performs signal reconstruction, in compliance to existing measurement standards. Even better performance than required by standards is achieved in transient conditions.
Preliminary results show High Level Synthesis approach can effectively model proposed problem. Compared to existing works, improvements in both speed and FPGA resource utilization are possible, which allows more precision algorithms in the future.



Segment of SVD algorithm using HLS in MATLAB

5. Conclusion and Future Work

Matrix decomposition algorithm speedup is crucial for real-time application of ESPRIT algorithm.
High level synthesis approach is suitable for tackling these multi-layer problems.
In future work, performance of the both the parametric dynamich phasor estimation approach and SVD decomposition algorithm will be evaluated and compared to existing works.

References

[1] Jian Song et al. - Accurate Dynamic Phasor Estimation by Matrix Pencil and Taylor Weighted Least Squares Method, IEEE Transactions on Instrumentation and Measurement 2021
[2] L. Stanitis et al. Optimization Techniques for Hestenes-Jacobi SVD on FPGAs, 2023 33rd International Conference on Field-Programmable Logic and Applications (FPL)

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