Bipolar Transistor Structures

Modern Si/SiGe Bipolar Transistors

Vertical current Super Self-aligned Transistors (SST)

SOI Lateral bipolar Transistors (LBT)

SST Structures - Advantages

Mainstream Si/SiGe bipolar technology, Optimized intrinsic region, high electrical performance:

<table>
<thead>
<tr>
<th></th>
<th>$f_T$, GHz</th>
<th>$f_{max}$, GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>54</td>
<td>65</td>
</tr>
<tr>
<td>SiGe</td>
<td>200-300</td>
<td>200-300</td>
</tr>
</tbody>
</table>

SiGe intrinsic base
SST Structures - Limitations

Large volume of parasitic regions:

- COLLECTOR CONTACT
- BASE CONTACT
- Emitter
- INT. EMITTER
- INT. COLLECTOR
- INT. BASE

A_{BE}/A_{CS}=1-4 \%,
high C_{BC}, C_{CS}, R_{B},
f_{T}(f_{L}),
complicated technology.

Scaling limitations due to the vertical current flow:
trench isolation, perimeter depletion effect

Lateral Bipolar Transistors (LBT)

Silicon-on Insulator (SOI) LBT

SOI LBT:
- Simple technology,
- Reduced capacitances,
- Compatible with thin-body silicon SOI CMOS technology.

\begin{tabular}{|c|c|}
\hline
f_{T}, GHz & f_{max}, GHz \\
\hline
LBT & 3-16 & 15-67 \\
\hline
\end{tabular}

High f_{max} \Rightarrow reduced C_{BC}.
Low f_{T} \Rightarrow wide base, unoptimized geometry and doping profile.

Low-power and/or SOI BICMOS applications.
A novel Horizontal Current Bipolar Transistor (HCBT) is introduced:

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Advantages:
- optimized doping profiles,
- low $C_{BC}$ and $C_{CS}$,
- scaling possibilities,
- simple technology:
  - single poly,
  - no epitaxy, no buried layer,
  - 5 masks,
  - no trench processing,
  - reduced etch and high-temp. steps,

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HCBT Technology

- 0.5 $\mu$m - lithography resolution,
- 0.1 $\mu$m - alignment margins.

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<110> wafer as substrate
- $n$-hill implantation,
- annealing,
- buffer oxidation,
- nitride deposition,

1st mask
- $n$-hill etching – RIE + TMAH,
- $P$-channel stopper implantation,

<111> defect-free, smooth sidewalls
HCBT Technology (cont’d)

- CVD oxide deposition,
- Densification,
- Chemical-mechanical Planarization (CMP),
- Etch-back
  
  \[ n\text{-hills are separated by isolation oxide,} \]
  
  \[ h_T: \text{active transistor height.} \]

HCBT Technology (cont’d)

- Extrinsic base implantation, 30°,
- Intrinsic base implantation, -40°,
- Polysilicon deposition,
- CMP

\[ 2^{nd} \text{mask} \]
HCBT Technology (cont’d)

HCBT key process parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>HCBT A</th>
<th>HCBT B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active height, $h_T$</td>
<td>0.52 $\mu$m</td>
<td>0.75 $\mu$m</td>
</tr>
<tr>
<td>Emitter height x length</td>
<td>$0.21 \times 5 \mu$m$^2$</td>
<td>$0.38 \times 5 \mu$m$^2$</td>
</tr>
<tr>
<td>Collector I/I dose, $@200$keV</td>
<td>$6 \times 10^{13}$ cm$^{-2}$</td>
<td>$4.5 \times 10^{13}$ cm$^{-2}$</td>
</tr>
<tr>
<td>Collector annealing, $N_2$</td>
<td>1050°C, 150'</td>
<td>-</td>
</tr>
<tr>
<td>Channel stopper I/I, 0°</td>
<td>BF$_2$, $6 \times 10^{13}$ cm$^{-2}$</td>
<td>-</td>
</tr>
<tr>
<td>Int. base I/I, BF$_2$</td>
<td>$3 \times 10^{13}$ cm$^{-2}$, 20keV, 35°</td>
<td>$2.3 \times 10^{13}$ cm$^{-2}$, 33keV, 30°</td>
</tr>
<tr>
<td>Base annealing, RTA</td>
<td>1050°C, 30°</td>
<td>900°C, 30°</td>
</tr>
</tbody>
</table>
HCBT Technology

Scaled HCBT is successfully processed in <110> wafers

- N-hill width: 0.58 µm
- Extrinsic base width: <0.3 µm
- Emitter height \( h_E \): 0.38 µm

HCBT Electrical Characteristics

Gummel plots of a typical HCBT structure

- Base current ideality factor ≈ 1
- Low-defect-density sidewalls,
- High quality interface with isolation oxide

Max. current gain = 75
HCBT Electrical Characteristics

Output characteristics of HCBT structure

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BV_{CEO}$ (V)</td>
<td>10.8</td>
</tr>
<tr>
<td>$BV_{CEO}$ (V)</td>
<td>5.6</td>
</tr>
<tr>
<td>$V_C$ (V), $I_B$=5 $\mu$A</td>
<td>7.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{re}$ (fF) @ 0 V</td>
<td>16</td>
</tr>
<tr>
<td>$C_{re}$ (fF)</td>
<td>18</td>
</tr>
<tr>
<td>$R_g$ (Ω) circle</td>
<td>120</td>
</tr>
<tr>
<td>$R_e$ (Ω)</td>
<td>63</td>
</tr>
<tr>
<td>$R_e$ (Ω), saturation</td>
<td>530</td>
</tr>
</tbody>
</table>

HCBT Electrical Characteristics

$f_t$ and $f_{max}$ vs. $I_C$ of HCBT Structure

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak $f_t$ (GHz), $V_{CE}$=5 V</td>
<td>23.5</td>
</tr>
<tr>
<td>Peak $f_{max}$ (GHz), $V_{CE}$=5 V</td>
<td>36</td>
</tr>
<tr>
<td>$I_B$ @ peak $f_t$ (mA)</td>
<td>165</td>
</tr>
<tr>
<td>$f_{TBV_{CEO}}$ (GHzV)</td>
<td>131.6</td>
</tr>
</tbody>
</table>
HCBT Process Analysis - \( \text{N}-\)hill Etching

**Sidewall roughness**

- Horizontal roughness
- Vertical roughness
- RIE etch profile

**Time multiplexed DRIE process**

**Photoresist edge roughness**

**Mass transport of etched species**

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HCBT Process Analysis - \( \text{N}-\)hill Etching

**Lithography optimization for sidewall roughness minimization**

**Unoptimized Lithography**

- Hardbake: 130 °C, 6'.
- no descum, 3000 rpm.
- 6-05-a1

**Optimized Lithography**

- Hardbake: 150 °C, 5'.
- descum, 5000 rpm.
- 6-18-51

*Hardbake cannot be afforded in every process; still not perfectly flat*
HCBT Process Analysis - N-hill Etching

Roughness by lithography and DRIE optimization: ≈10-80 nm,
Base width of HCBT: ≈60-150 nm,
Emitter depth: ≈20-50 nm.

Still too rough for high-performance bipolar and MOS transistors!!

Solution: Usage of Crystallographic etches (e.g. KOH, TMAH, EDP):

• High selectivity between <111> and <100> crystal planes: from 60:1 to 120:1.

• The usage of <110> wafers: <111> plane is perpendicular to surface.

HCBT Effects Analyses

HCBT n-collector doping:

Collector doping process:
4.5·10^{13} cm^{-2}, 200keV implant.
1050°C, 150 min. annealing.

- High collector doping:
  - Kirk effect pushed to higher currents,
  - high $f_T$.
**HCBT Simulation Analyses**

*High breakdown achieved despite high collector doping:*

Collector-base electric field shielding by extrinsic base

**HCBT narrow ext. base**
- Lower breakdown voltage

**HCBT long ext. base**
- Higher breakdown voltage

**E-field of HCBT structure with and without ext. base:**

*Peak E-field reduced in HCBT with ext. base:*
- Shielding effect
- Lower impact ionization rate
- Increased $BV_{CEO}$
**HCBT Simulation Analyses**

**Maximum E-field of HCBT structure vs. ext. base width:**

Peak E-field reduced for ext. base width \( w_{\text{ext}} > 0.3 \mu m \)

The larger \( w_{\text{ext}} \), the larger max. \( E \)-field => Increased \( BV_{CEO} \) by 1.7 V

**Old HCBT Process: (1 \( \mu m \) / 1 \( \mu m \)) Technology:**

\( f_T \) and \( f_{\text{max}} \), limited by the wide ext. base.

\( V_{CE} = 2 \) V
\( V_{CE} = 6 \) V
\( V_{CE} = 10 \) V

\( V_{BE} = 0.1 \) V
HCBT Process Scaling

Reduction of $n$-hill and extrinsic base widths should improve HCBT characteristics:

**Scaling**

- **$N$-hill width:** 5 $\mu$m
- **Extrinsic base width:** 5 $\mu$m
- **$f_T$:** 4.2 GHz
- **$f_{max}$:** 12 GHz
- **$BV_{CEO}$:** 15.5 V
- **$f_{T,BV_{CEO}}$:** 65.1 GHzV

$<1 \mu$m

$<0.5 \mu$m

23.5 GHz

35 GHz

5.6 V

131.6 GHzV


HCBT vs. SOI LBTs

**HCBT vs. SOI Lateral Bipolar Transistors (LBT):**

**HCBT:**

- The highest absolute $f_T$ (23.5 GHz), and $f_{T,BV_{CEO}}$ (131.6 GHzV)!!

**Among SOI LBTs**


Department of Electronics, Microelectronics, Computer and Intelligent Systems
HCBT vs. SST BJT’s

HCBT vs. vertical-current Super Self-Aligned bipolar Transistors (SST)

HCBT: Comparable with state-of-art Si BJT’s !!

HCBT Characteristics can be improved further by using SiGe base !!