Hrvatska sekcija IEEE, Odjel za elektroničke elemente / poluvodičke integrirane sklopove pozivaju vas na:

Distinguished Lecturers' Day

U okviru kojeg će se odžati predavanja tri istaknuta predavča IEEE Društva za poluvodičke integrirane sklopove (SSCS Distinguished Lecturers): Jan Craninckx, *IMEC*; Franz Dielacher, *Infineon*; i Yorgos Palaskas, *Intel*.

Predavanja će se održati u **petak, 13. rujna 2013.** u Sivoj Vijećnici FER-a prema rasporedu:

9:00	Uvod
9:10	Jan Craninckx, *Low-power Successive Approximation ADCs for Wireless Applications*
10:30	Franz Dielacher, *Circuit Design in SiGe:C for Microwave Links and Active Safety Systems*
11:45	Pauza za kavu
12:15	Yorgos Palaskas, *Scaling-friendly Radio Design for SoC*

Sadržaje predavanja i životopise predavača pročitajte u nastavku obavijesti.

Low-power Successive Approximation ADCs for Wireless Applications

Abstract:
This talk discusses the advancements made in SAR ADCs for wireless applications, which require accuracies in the range of 8-10bit and a few 10's of MHz sampling speed. An overview is given of recent techniques that reduce the switching power in the capacitive DAC, and as such improve the power efficiency of the ADC up to levels that are out of reach of the typically used pipeline architecture.
The second part of this paper discusses some specific state-of-the-art designs. The charge-sharing SAR ADC architecture is introduced, which proposes a new signal processing method in the charge domain that removes the often-neglected though requirements for the reference buffer. A high-speed design that combines time-interleaving, pipelining and SAR techniques achieves 10 ENOB and 250MS/s at a figure of merit of 10fJ.

Bio:
Jan Craninckx obtained his Ms. and Ph.D. degree in microelectronics *summa cum laude* from the ESAT-MICAS laboratories of the Katholieke Universiteit Leuven in 1992 and 1997, respectively. His Ph.D. work was on the design of low-phase noise CMOS integrated VCOs and synthesizers.
From 1997 till 2002 he worked with Alcatel Microelectronics (later part of ST Microelectronics) as a senior RF engineer on the integration of RF transceivers for GSM, DECT, Bluetooth and WLAN. In 2002 he joined IMEC (Leuven, Belgium), where he currently is the senior principal scientist of the analog wireless research group. His research focuses on the design of RF transceiver front-ends for software defined radio (SDR) systems, covering all aspects of RF, analog and data converter design.
Dr. Craninckx has authored and co-authored more than 100 papers and several book chapters, and is the inventor of 10 patents. He is a member of the Technical Program Committee for the several conferences, was the chair of the SSCS Benelux chapter (2006-2011), and is an Associate Editor of the JSSC.

Circuit Design in SiGe:C for Microwave Links and Active Safety Systems

Abstract:
Low-cost (silicon- based) mass market exploitation of large amounts of bandwidth at 60 GHz and above can be foreseen over the next decade for areas like wireless-connectivity, sensor networks, car-radar, identification and e-safety.
In its introduction, the presentation will give a summary of the challenges and requirements in the context of technology selection and system partitioning. Advanced packaging technologies with embedded passive components and package co-design will be addressed too.
For the circuit design itself new efficient millimeter-wave radios and transceiver concepts will be explored and design issues will be described. Finally some examples for highly integrated MMIC solutions for applications like car guidance and active safety systems and for high data-rate outdoor (E-band) communications will be given.

Bio:

Franz Dielacher received his M.S. and Ph.D. degrees in electrical engineering from the Graz University of Technology, Austria. His doctoral research was directed towards the modeling, simulation and design of oversampled analog-to-digital converters.

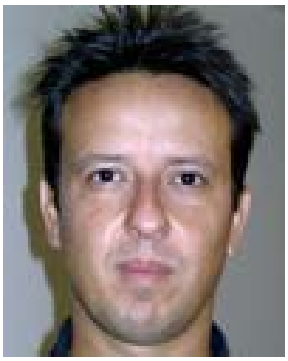
From 1981 until 1999 he worked for Siemens Semiconductor Group in circuit development and system integration for wireline and wireless communications. Since 1999 Dr. Dielacher is with Infineon Technologies in various positions in circuits and systems for communications like DSL, high-speed transceivers, and wireless infrastructure. Currently he is a Senior Principal Engineer and Chief Scientist in the RF-Power Group.

His international involvement includes ISSCC TPC member from 2001 to 2011, ISSCC wireline subcommittee chair, ESSCIRC TPC member, ESSCIRC technical program committee chair in 2001, ESSCIRC steering board member and IEEE SSCS AdCOM member since 2011.

Scaling-friendly Radio Design for SoC

Abstract:

Integration of RF together with baseband and possibly application processors in a System-on-Chip is appealing for cost and form-factor reasons. Conventional radios are generally incompatible with SoC: they do not scale well with CMOS process and typically require long development times (respins, accurate RF models, etc). Scaling-friendly radios, on the other hand, introduce fundamentally different ways of radio operation, e.g. encode information in the phase rather than the amplitude of the signal. This results in improving resolution and performance with CMOS scaling due to the faster transistors. Circuit behavior might now be adequately described with a basic *digital* MOS model, improving time-to-market. Advanced DSP and digital calibration integrate seamlessly with the radio to further enhance the performance. Finally the digital nature of such systems enables substantial flexibility that can be beneficial e.g. for multi-comm operation. The talk will present case studies demonstrating the potential of such scaling-friendly radio concepts. For example, a digital 32nm WiFi transmitter will be presented that is based on high resolution, digitally-controlled delay cells that introduce the modulation. The transmitter includes a switching power amplifier that was designed with no RF models and still achieved competitive efficiency and excellent linearity. Finally a reconfigurable all-digital system is presented for flexible multi-comm LO generation. Presented scaling-friendly radio systems achieve compelling performance already in 32nm CMOS and are expected to further improve with CMOS scaling, almost on par with digital circuits.



Bio:

Yorgos Palaskas (S'98, M'02, SM'11) received the Diploma in Electrical and Computer Engineering from the National Technical University of Athens, Greece, in 1996, and the M.S. and Ph.D. degrees, both in Electrical Engineering, from Columbia University, New York, in 1999 and 2002, respectively.

Since 2003 he has been with Intel Labs, Hillsboro, Oregon, where he is currently a Principal Engineer. During 2003-2005 he worked on integrated MIMO transceivers and power amplifiers for WiFi. Since 2006 he has been leading research projects on scaling-friendly, SoC compatible, 4G/WiFi radios in heavily scaled CMOS processes, and also research on 60GHz radios for multi-Gb/s wireless communications. He has authored and co-authored more than 40 papers at IEEE journals and conferences, 1 book chapter, and has 20 patents issued and several pending. He served on the TPC for the IEEE International Solid-State Circuits Conference 2009-2013, and is currently serving on the TPC for the IEEE European Solid-State Circuits Conference.